What is claimed:

1. A method for manufacturing a semiconductor device, the method comprising:

(a) forming a gate dielectric layer over a semiconductor substrate;

(b) forming a gate electrode over the gate dielectric layer;

(c) forming an extension control layer over the semiconductor substrate on sides of the gate dielectric layer; and

(d) forming a first impurity layer and a second impurity layer by ion-implanting an impurity in the semiconductor substrate,

wherein an extension region is formed in the semiconductor substrate below the extension control layer during the ion-implanting used to form the first impurity layer and the second impurity layer.

2. A method for manufacturing a semiconductor device according to claim 1, wherein the step (c) further includes the step of forming a sidewall protection film on sidewalls of the gate electrode with the extension control layers.

3. A method for manufacturing a semiconductor device according to claim 2, wherein the step (c) further includes the steps of:

(c – 1) forming a dielectric layer over the semiconductor substrate; 112 1st paragraph

(c – 2) forming a sidewall mask layer on sides of the gate electrode over the dielectric layer;

(c – 3) removing the dielectric layer using the sidewall mask layer as a mask to form the extension control layer and the sidewall protection layer; and

(c – 4) removing the sidewall mask layer after the step (c – 3).

4. A method for manufacturing a semiconductor device according to claim 3, wherein the extension control layer is formed from a material comprising silicon nitride.

5. A method for manufacturing a semiconductor device according to claim 4, wherein the sidewall mask layer is formed from a material comprising silicon oxide.

6. A method for manufacturing a semiconductor device according to claim 3, wherein the extension control layer is formed from a material comprising silicon oxide.

7. A method for manufacturing a semiconductor device according to claim 6, wherein the sidewall mask layer is formed from a material comprising silicon nitride.

8. A method for manufacturing a semiconductor device according to claim 1, wherein the extension control layer has a thickness of 5 – 50 nm.

9. A method for manufacturing a semiconductor device according to claim 3, wherein the sidewall mask layer is formed to a thickness of 30 – 200 nm.

10. A semiconductor device comprising:
a gate dielectric layer provided over a semiconductor substrate;
a gate electrode provided over the gate dielectric layer;
a first impurity layer and a second impurity layer provided in the semiconductor substrate and spaced away from sides of the gate dielectric layer;
an extension region provided in the semiconductor substrate between the gate dielectric layer and at least one of the first impurity layer and the second impurity layer; and
an extension control layer provided over the extension region.

11. A semiconductor device according to claim 10, further comprising a sidewall protection film formed on sidewalls of the gate electrode.

12. A semiconductor device according to claim 11, wherein the sidewall protection film comprises silicon oxide and the extension control layer comprises silicon nitride.

13. A semiconductor device according to claim 11, wherein the sidewall protection film comprises silicon nitride and the extension control layer comprises silicon oxide.

14. A semiconductor device according to claim 11, wherein the sidewall protection film is integral with the extension control layer.

15. A semiconductor device according to claim 11, wherein the extension control layer and the sidewall protection film define a substantially L-shaped cross-sectional configuration.

16. A semiconductor device according to claim 10, wherein the extension control layer comprises silicon nitride.

17. A semiconductor device according to claim 10, wherein the extension control layer comprises silicon oxide.

18. A semiconductor device according to claim 10, wherein the extension control layer has a thickness of 5 – 50 nm.

19. A semiconductor device according to claim 10, wherein the extension region includes portions provided in the semiconductor substrate between the gate dielectric layer and both the first impurity layer and the second impurity layer.

20. A semiconductor device according to claim 19, further comprising a sidewall protection film on sidewalls of the gate electrode, wherein the extension control layer and sidewall protection film form a substantially L-shaped structure in cross section on at least one side of the gate dielectric layer.

21. A method for manufacturing a semiconductor device including extension regions and source/drain regions formed using a single ion-implantation step, the method comprising:

forming a gate dielectric layer over a semiconductor substrate;

forming a gate electrode over the gate dielectric layer;

forming extension control structures over a portion of the semiconductor substrate next to the gate dielectric layer; and

a single ion-implanting step that forms extension regions in the semiconductor substrate under the extension control structures and source/drain regions in the semiconductor substrate adjacent to the extension layer, wherein the extension regions have a depth that is less than that of the source/drain regions.

22. A method according to claim 21, further comprising forming sidewall protection structures on sidewalls of the gate electrode, wherein the sidewall protection structures are formed from the same material as the extension control structures.

23. A method according to claim 22, wherein the extension control structures and sidewall protection structures are formed using a method comprising:

depositing a dielectric layer over the surface of the semiconductor substrate and the gate electrode;

forming a mask layer on the dielectric layer;

anisotropically etching the mask layer to form a sidewall mask layer;

etching the dielectric layer using the sidewall mask layer as a mask so that the dielectric layer remains at sidewalls of the gate electrode and extends a distance outward from the gate dielectric layer along the surface of the dielectric layer; and

removing the sidewall mask layer;

wherein the dielectric layer remaining at sidewalls of the gate electrode defines the sidewall protection structures and the dielectric layer extending a distance outward from the

gate dielectric layer along the surface of the dielectric layer defines the extension control structures.

24. A method of manufacturing a semiconductor device according to claim 1, wherein the extension control layer is formed from a dielectric material.